St. JOSEPH'S DEGREE COLLEGE

Sunkesula Road, Kurnool – 518 004 A.P.

(Affiliated to Rayalaseema University, Kurnool)

Workshop

on

"Digital Logic Design"

By

Mr.K.Subash Chandra Naidu **M.Sc, B.Ed**

Lecturer

Department of Electronics, St. Joseph's Degree College, KURNOOL.

Academic Year 2023-2024

Faculty Attended

Computer science department

Faculty members of various degree colleges

Rayalseema University, Kurnool

Course Co-ordinators:

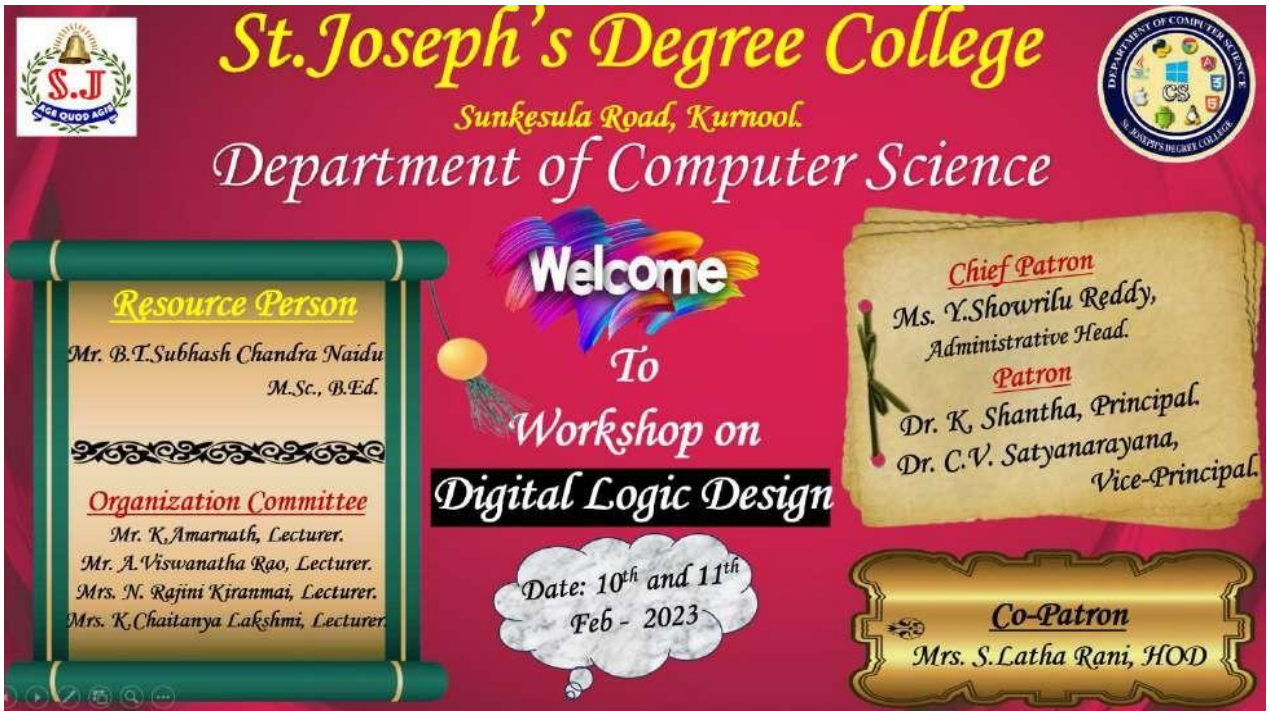
Mr. K. Amarnath **Mr. A.Viswanatha Rao**

CIRCULAR

05-02-2024,
Kurnool.

Computer Science Department, St. Joseph's Degree College planning to organize a 2-Day workshop on "**Digital Logic Design**" by Mr. Subash Chandra Naidu, Lecturer, Department of Electronics, St. Jospeh's Degree College. Kurnool.

(S Latha Rani)
Head, Computer Science Department.



2-Days Work Shop on Digital Logic Design

Work shop is a powerful peer assessment activity to discuss and perform practical work in a subject or an activity. It is structured and interactive session designed to create an environment for meaningful work and to guide a group through a process that will lead to great outcomes.

Computer Science Department organized a 2-Day workshop on Digital Logic Design in order to enhance, engage the faculty to foster their ability in DLD.

Mr. K.Subash Chandra Naidu, Lecturer, Kurnool was the right person to do so. The main objective of the workshop is to learn DLD practically using electronic equipment as DLD got introduced in curriculum for this academic year.

Dates: 10th,11th Feb 2024.

Time: 9am – 5pm.

Place: Lab2, Building 2, St.Joseph's Degree College.

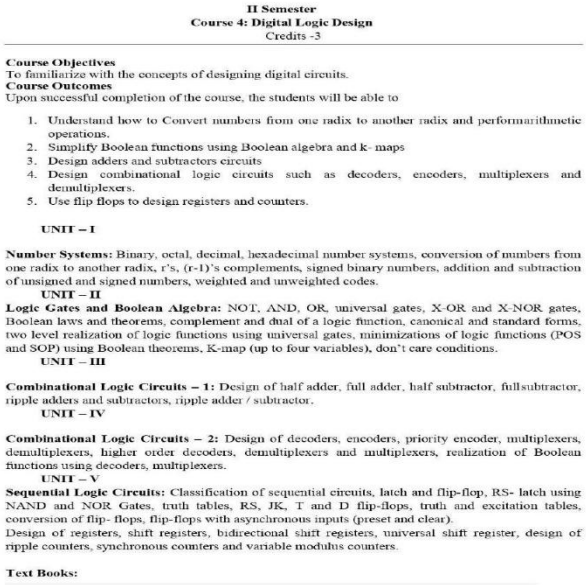
Topic:Digital Logic design

Resource person: Mr. K.SubashChandra Naidu,

Designation: Lecturer, Department of Electronics, St. Jospeh's Degree College. Kurnool.

OUTCOME:

- To learn various types of number systems and their conversions.
- To simplify the Boolean expression and apply the Boolean theorems through logical gates.
- To design and implement variety of logical devices using combinational circuits concepts.
- To Demonstrate and compare the construction of programmable logic devices and different types of ROM.
- To analyze sequential circuits like Registers and counters using flip-flops.



II Semester
Course 4: Digital Logic Design
Credits -3

Course Objectives
To familiarize with the concepts of designing digital circuits.
Course Outcomes
Upon successful completion of the course, the students will be able to

1. Understand how to Convert numbers from one radix to another radix and performarithmetic operations.
2. Simplify Boolean functions using Boolean algebra and k- maps
3. Design adders and subtractors circuits
4. Design combinational logic circuits such as decoders, encoders, multiplexers and demultiplexers.
5. Use flip flops to design registers and counters.

UNIT – I

Number Systems: Binary, octal, decimal, hexadecimal number systems, conversion of numbers from one radix to another radix, r's, (r-1)'s complements, signed binary numbers, addition and subtraction of unsigned and signed numbers, weighted and unweighted codes.

UNIT – II

Logic Gates and Boolean Algebra: NOT, AND, OR, universal gates, X-OR and X-NOR gates, Boolean laws and theorems, complement and dual of a logic function, canonical and standard forms, two level realization of logic functions using universal gates, minimizations of logic functions (POS and SOP) using Boolean theorems, K-map (up to four variables), don't care conditions.

UNIT – III

Combinational Logic Circuits – 1: Design of half adder, full adder, half subtractor, fullsubtractor, ripple adders and subtractors, ripple adder / subtractor.

UNIT – IV

Combinational Logic Circuits – 2: Design of decoders, encoders, priority encoder, multiplexers, demultiplexers, higher order decoders, demultiplexers and multiplexers, realization of Boolean functions using decoders, multiplexers.

UNIT – V

Sequential Logic Circuits: Classification of sequential circuits, latch and flip-flop, RS- latch using NAND and NOR Gates, truth tables, RS, JK, T and D flip-flops, truth and excitation tables, conversion of flip- flops, flip-flops with asynchronous inputs (preset and clear).
Design of registers, shift registers, bidirectional shift registers, universal shift register, design of ripple counters, synchronous counters and variable modulus counters.

Text Books:

Agenda

OBJECTIVES:

- To familiarize with the concepts of designing digital circuits.
- To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits.
- To prepare participants to perform the analysis and design of various digital electronic circuits.

OUTCOME:

After this workshop, the participants would gain enough knowledge

- Have a thorough understanding of the fundamental concepts and techniques used in digital electronics.
- To understand and examine the structure of various number systems and its application in digital design.
- The ability to understand, analyze and design various combinational and sequential circuits.
- The ability to identify and prevent various hazards and timing problems in a digital design.
- To develop skill to build, and troubleshoot digital circuits.

Program – Day- I:

Time	Activity	Remarks
08.45 am	Arrival of participants	
9.00 am to 9.30 am	Inviting guests on to the Dias	
	Prayer Song	
	Welcome Note and presentation of workshop program and objectives	By Mr. **K.Amarnath**
	Opening Remarks	By **Mrs.S.Latha Rani, HOD**
	Address by Vice Principal Dr.**C.V.Satyanarayana**	
	Address by Principal Dr. **K.Shantha**	
09:30 am to 11.00 am	Session – I	
11.00 am to 11.15 am	**Tea Break**	
11.15 am to 1.00 pm	Session –II	
1:00 pm to 2:00 pm	**Lunch Break**	
2.00 pm to 3:30 pm	Session –III	Demo of Practical implementation
3.30 pm to 3.45 pm	**Tea Break**	
3.45 pm to 5.00 pm	Session – IV & End of Day – I	Practical implementation by participants

Program – Day – II :

Time	Activity	Remarks

09:00 am to 11.00 am	Session – I	
11.00 am to 11.15 am	***Tea Break***	
11.15 am to 1.00 pm	Session –II	Practical implementation by Participants
1:00 pm to2:00 pm	**Lunch Break**	
2.00 pm to 4.00 pm	Valedictory & closing ceremony	

SYLLABUS

DAY 1 Morning Session:

- Signed binary numbers, addition and subtraction of unsigned and signed numbers.
- Weighted and unweighted codes.
- NOT, AND, OR, universal gates, X-OR and X-NOR gates.
- Boolean laws and theorems, complement and dual of a logic function.
- Canonical and standard forms.

Afternoon Session:
Practicals:

- Introduction to Electronic breadboard, Integrated Circuits (Logic gates) like AND, OR NOT, XOR
- PIN configuration of logic gates. Testing of basic Logic gates.

DAY 2: Morning Session:

- Two level realization of logic functions using universal gates.
- Minimizations of logic functions (POS and SOP) using Boolean theorems. □ K-map (up to four variables).
- Don't care conditions.

Afternoon Session:

Practicals:

- Design of half adder and Half subtractor

ATTENDANCE SHEETS

St.Joseph's Degree College, Sunkesula Road, Kurnool
Workshop on "Digital Logic Design" 10th & 11th February , 2024
Online Attended Participants Details

Sno	Name of the Faculty	College	Mobile	Email id
1	S Bhaskara Naik Dr M SreeDevi	SVB Govt Degrees college	8309827895	baskarnaik808@gmail.com
2	Associate professor Sv University Tirupati	Sv University , Tirupati	8309827895	baskarnaik808@gmail.com
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4	Noya Hussain	Dr Jothimmy Degeree college adoni	8184855847	hunain.boya@gmail.com
5	Yenniguruu Lakshmi Kavitha gouda	SSAGovt Degree,college -Ballari	9620177901	kavitha816@gmail.com
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7	D PULLAIAH	Kvsr degree college Allagadda	7893182236	pullaiah786@gmail.com
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13	C BADULLA	National Degree College Nandyal	9885619553	badullansc@gmail.com
14	M. MALATHI	Ravindra degree college for women	9703062465	malathi.kvrmhan@gmail.com
15	MAHAMMAD RAFI. B	NATIONAL DEGREE COLLEGE, NANDYAL	9866449900	rafimail73@gmail.com
16	SAQUA ZAREEN	St.Joseph's Degree College	9030917408	saquarasha10@gmail.com
17	Maddun Joyce	St.Joseph's Degree College	9951741676	joycemaddun1234@gmail.com
18	K Vanitha kumari	St.Joseph's degree college kurnool	7306565096	kmanavanitha@gmail.com
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20	S AFSHAN ANJUM	St Joseph's Degree College	9032347923	shaikafsharjum@gmail.com
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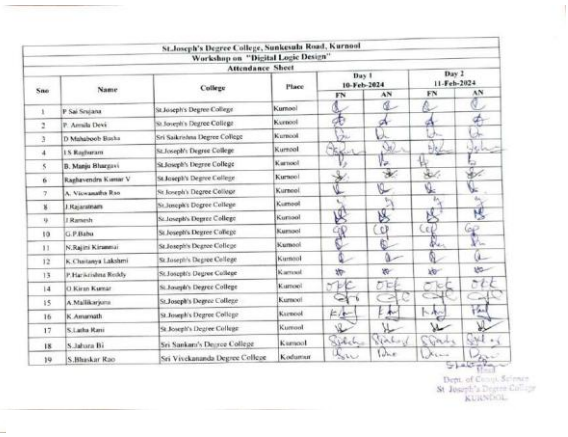
23	M.Usha	Vyshnavi Degree College, Yemmiganur	9705975815	ushasri196@gmail.com
24	Dr.M.Balasubramanyam	SRI RAMAKRISHNA DEGREE COLLEGE NANDYAL	6304033063	mbalasubramanyam4@gmail.com

Head
Dept. of Comp. Science
St Joseph's Degree College
KURNOOL



St.Joseph's Degree College, Sunkesula Road, Kurnool
Workshop on "Digital Logic Design"
Attendance Sheet

Sno	Name	College	Place	Day 1 10-Feb-2024		Day 2 11-Feb-2024	
				FN	AN	FN	AN
1	P Sai Srujana	St.Joseph's Degree College	Kurnool				
2	P. Amala Devi	St.Joseph's Degree College	Kurnool				
3	D Mahaboob Basha	Sri Saikrishna Degree College	Kurnool				
4	I.S Raghuram	St.Joseph's Degree College	Kurnool				
5	B. Manju Bhargavi	St.Joseph's Degree College	Kurnool				
6	Raghavendra Kumar V	St.Joseph's Degree College	Kurnool				
7	A. Viswanadha Rao	St.Joseph's Degree College	Kurnool				
8	J.Rajasimam	St.Joseph's Degree College	Kurnool				
9	J.Ramesh	St.Joseph's Degree College	Kurnool				
10	G.P.Babu	St.Joseph's Degree College	Kurnool				
11	N.Rajini Kiranmai	St.Joseph's Degree College	Kurnool				
12	K.Chaitanya Lakshmi	St.Joseph's Degree College	Kurnool				
13	P.Harikrishna Reddy	St.Joseph's Degree College	Kurnool				
14	O.Kiran Kumar	St.Joseph's Degree College	Kurnool				
15	A.Mallikarjuna	St.Joseph's Degree College	Kurnool				
16	K.Amarnath	St.Joseph's Degree College	Kurnool				
17	S.Latha Rani	St.Joseph's Degree College	Kurnool				
18	S.Jahara Bi	Sri Sankari's Degree College	Kurnool				
19	S.Bhaskar Rao	Sri Vivekananda Degree College	Kodumur				

Dept. of Comp. Science
St Joseph's Degree College
KURNOOL

FEEDBACK

- Faculty members of Computer Science Departments, Rayalaseema University Affiliated Colleges.
- TotalNo.ofParticipantsRegistered: **43**
- TotalNo.ofParticipants Attended: **43**

GoogleDriveLinkforRegistrationforms:

https://forms.gle/6ZRSwAueXQWNzgfX8

GoogleDriveLinkforFeedback forms:

https://forms.gle/AEoSAJucfKEya7NT8

GALLERY


CERTIFICATE